

ABSTRACT OF THE DISCLOSURE

The invention provides a PLL circuit wherein, even if the duty ratio of an input signal varies, stabilized PLL operation is achieved. The PLL circuit includes a phase detection circuit and a frequency detection circuit. The frequency detection circuit includes a pair of D-type flip-flops for sampling first and second clock signals having different phases from each other in synchronism with an input signal at each rising or falling changing point of the input signal for each period, and a control logic circuit for logically operating the signals sampled by the D-type flip-flops and the signals sampled successively subsequently by the D-type flip-flops. The control logic circuit generates an UP pulse signal or a DOWN pulse signal based on a result of the arithmetic operation.